

# Abstracts

## **A 1.5-V 4-GHz dynamic-loading regenerative frequency doubler in a 0.35-/spl mu/m CMOS process (2002 Vol. I [MWSYM])**

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*J.M.C. Wong and H.C. Luong. "A 1.5-V 4-GHz dynamic-loading regenerative frequency doubler in a 0.35-/spl mu/m CMOS process (2002 Vol. I [MWSYM])." 2002 MTT-S International Microwave Symposium Digest 02.1 (2002 Vol. I [MWSYM]): 573-576 vol. 1.*

This paper proposes a new topology of a frequency doubler using a dynamic-loading technique to achieve higher operating frequency, larger output swing, larger bandwidth and lower phase noise compared to traditional designs. Implemented in a standard 0.35-/spl mu/m digital CMOS process and at a 1.5-V supply, the proposed frequency doubler measures a maximum operating output frequency of 4 GHz with a bandwidth of 2.4 GHz while consuming a power of 3.7mW. The single-ended output amplitude is ranging from -3.0 to -6.5 dBm, and the phase noise is as low as -111dBc/Hz @ 500kHz offset.

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